



WHM2060AE

2.0 – 6.0 GHz LOW NOISE WIDE BAND AMPLIFIER

REV E
February 2018

Key Features



- 50 Ohm Impedance
- 2.0 ~ 6.0 GHz
- 0.90 dB Noise Figure
- 22.0 dBm Output IP₃
- 26.0 dB Gain
- 12.0 dBm P_{1dB}
- 1.5:1 VSWR
- Single Power Supply
- RoHS Compliant
- Unconditional Stable, $k > 1$
- RoHS Compliant
- MSL-1 Moisture Sensitivity Level

Product Description

WHM2060AE is integrated with WanTcom proprietary low noise amplifier technologies, high frequency micro electronic assembly techniques, and high reliability designs to realize optimum low noise figure, wideband, and high performances together. With single +5.0V DC operation, the amplifier has optimal input and output matching in the specified frequency range at 50-Ohm impedance system. The amplifier has standard 0.35" x 0.25" x 0.090" surface mount package.

The amplifier is designed to meet the rugged standard of MIL-STD-883g.

CAUTION:



ELECTROSTATIC DISCHARGE SENSITIVE

Applications

- Mobile Infrastructures
- WiMAX
- Defense
- Security System
- Measurement
- Fixed Wireless



Specifications

Summary of the key electrical specifications at room temperature

Index	Testing Item	Symbol	Test Constraints	Min	Nom	Max	Unit
1	Gain	S ₂₁	2.0 – 6.0 GHz	24	26	28	dB
2	Gain Variation	ΔG	2.0 – 6.0 GHz		+/- 1.0		dB
3	Input VSWR	SWR ₁	2.0 – 6.0 GHz		1.5	1.8	Ratio
4	Output VSWR	SWR ₂	2.0 – 6.0 GHz		1.4	1.8	Ratio
5	Reverse Isolation	S ₁₂	2.0 – 6.0 GHz		42		dB
6	Noise Figure	NF	2.0 – 6.0 GHz		0.90	1.1	dB
7	Output Gain 1dB Compression Point	P _{1dB}	2.0 – 6.0 GHz	10	12		dBm
8	Output-Third-Order Interception Point	IP ₃	Two-Tone, P _{out} = 0 dBm each, 1 MHz separation		22		dBm
9	DC Current Consumption	I _{dd}	@ 21 °C		45		mA
10	DC Power Supply Voltage	V _{dd}		+4.7	+5.0	+5.3	V
11	Thermal Resistance	R _{th,c}	Junction to case, last stage transistor			220	°C/W
12	Operating Temperature	T _o	Case temperature at the bottom of the housing	-40		+85	°C
13	Maximum Input CW RF Power	P _{IN, MAX}	DC – 13 GHz			10	dBm
14	Spurious	P _{spur}	DC – 13 GHz	-70			dBc

Absolute Maximum Ratings

Parameters	Units	Ratings
DC Power Supply Voltage	V	6.0
Drain Current	mA	70
Total Power Dissipation	mW	400
Input CW RF Power	dBm	10
Junction Temperature	°C	150
Storage Temperature	°C	-65 ~ 150
Operating Temperature	°C	-40 ~ +85
Thermal Resistance	°C/W	220

Operation of this device beyond any one of these parameters may cause permanent damage.

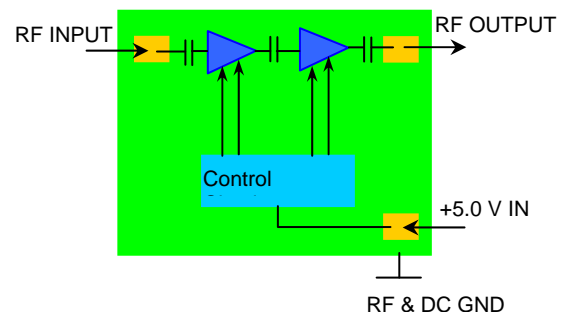
Ordering Information

Model Number	WHM2060AE
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ESD resistance tube of 20 pieces is used for the packing. Contact factory for tape and reel packing option for higher volume order.

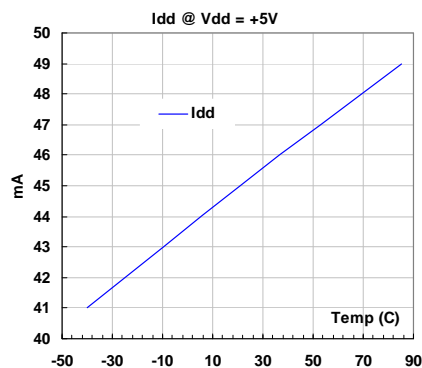
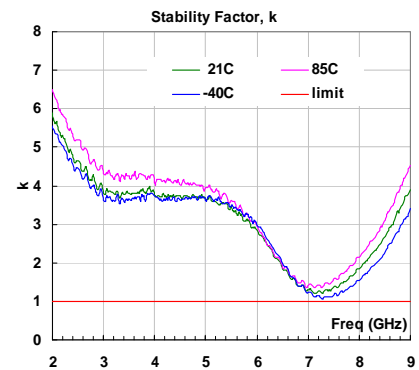
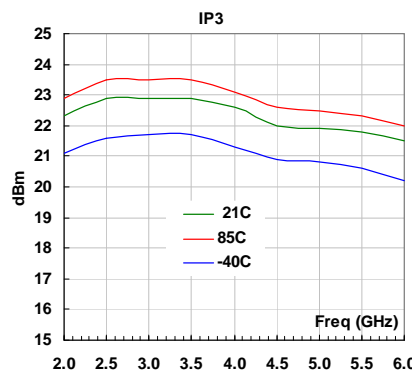
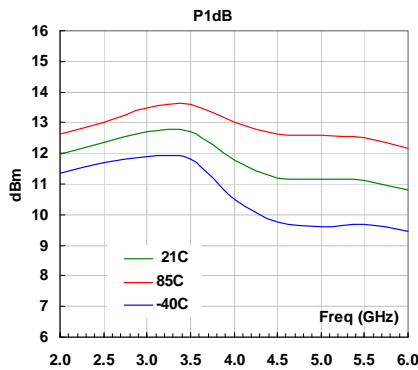
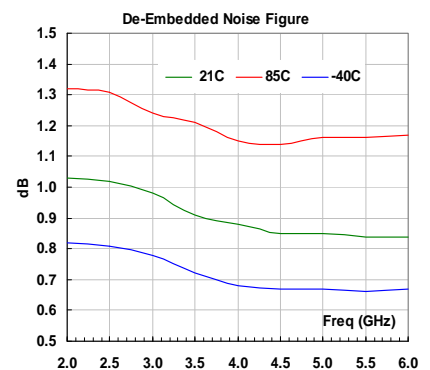
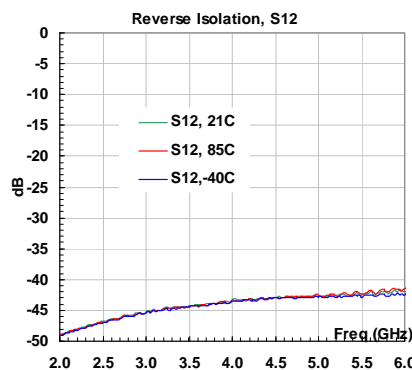
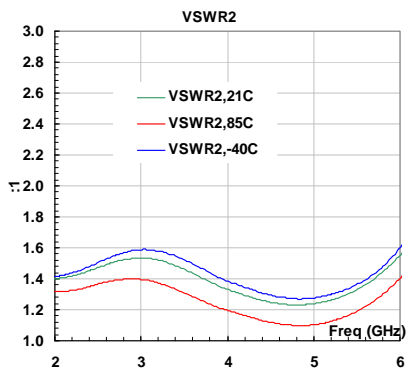
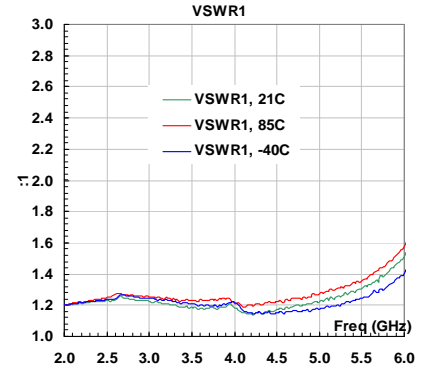
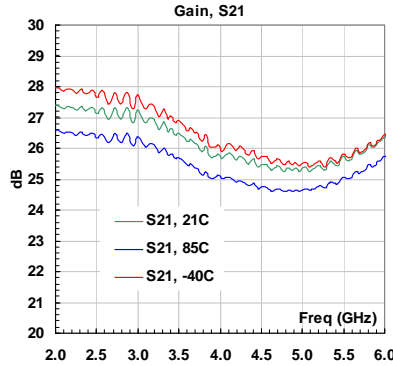
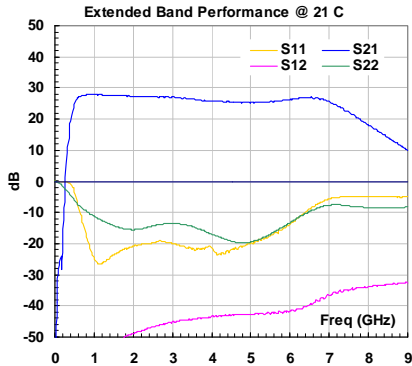
Specifications and information are subject to change without notice.

Functional Block Diagram





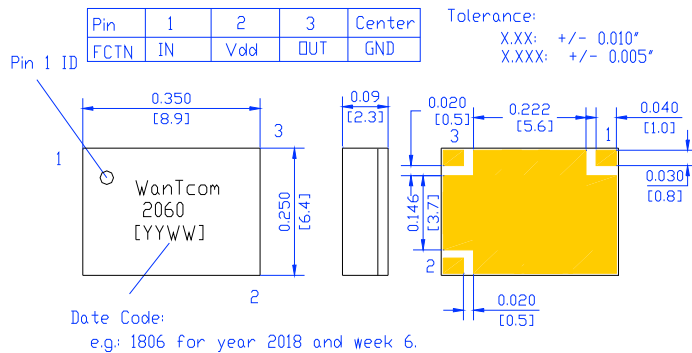
Typical Data



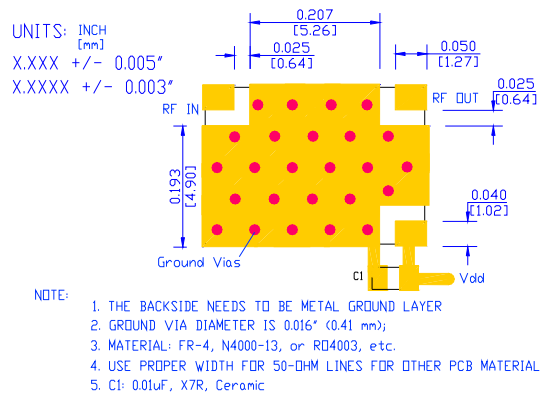
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Outline



Footprint



Application Notes:

A. Motherboard Layout

The recommended motherboard layout is shown in diagram of **Foot Print/Mounting Layout**. Sufficient numbers of ground vias on center ground pad are essential for the RF grounding. The width of the 50-Ohm microstrip lines at the input and output RF ports may be different for different property of the substrate. The ground plane on the backside of the substrate is needed to connect the center ground pad through the vias. The ground plane is also essential for the 50-Ohm microstrip line launches at the input and output ports.

The +5V DC voltage is applied at Pin 2. The 0.01 uF de-coupling capacitor, C₁, with minimum rating voltage of 10V is needed across the +5V pin to ground. The capacitor must be rated in the temperature range of -55 °C to 100 °C to ensure the entire circuit working in the specified temperature range.

No DC block capacitor is required at input and output RF ports. There are built-in DC block capacitors at the input and output.

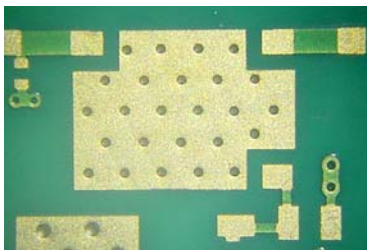


Fig. 1 Example of the motherboard

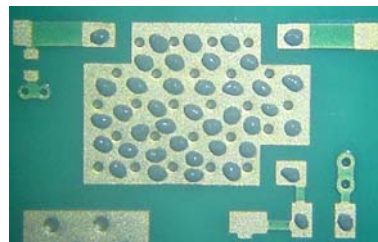


Fig. 2 Dispensed solder paste

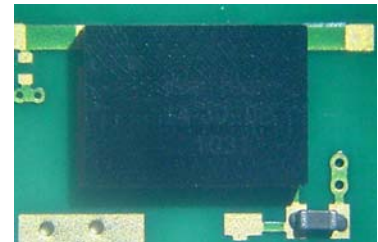


Fig. 3 Assembled part

B. Assembly

The regular low temperature and no clean solder paste such as SN63/Pb37 is recommended. The high temperature solder has been used internally for the WHM series amplifier assembly. The melting temperature point of the high temperature solder is around 240 °C. Thus, melting temperature of the solder paste should be below 220 °C for assembling WHM series amplifier on the test board to reduce the possible damage. The temperature melting point of the SN63/Pb37 solder paste is around 183 °C and is suitable for the assembly purpose. For RoHs compliance requirement, the 60Sn/40Bi Pb free low temperature solder paste should be used.

The reflow process using the regular SAC305 RoHs compliant solder paste will damage the amplifier due to the peak reflow temperature exceed 240 °C!



The SN63/Pb37 solder paste can be dispensed by a needle manually or driven by a compressed air. **Figure 2** shows the example of the dispensed solder paste pattern. Each solder paste dot is in the diameter of 0.005" ~ 0.010" (0.125 ~ 0.250 mm).

For volume assembly, a stencil with 0.004" (0.10 mm) is recommended to print the solder paste on the circuit board.

For more detail assembly process, refer to AN-109 at www.wantcominc.com website.

C. Electrical Testing and Fine Tuning

The amplifier is designed to be fully matched at the input and output ports. Any tuning is not needed. However, when connecting the assembled amplifier to a device such as a SMA connector or a filter, the connecting point or joint point could affect mainly the return loss at the port due to the non-ideal 50-Ohm impedance of the device. By varying the connection feature size such as the solder amount to get the optimum return loss or best matching result at the interface. This fine-tuning has little affect on the other performance such as gain, noise figure, P_{1dB} , or IP_3 .

During the fine-tuning process, a vector network analyzer can be used to monitoring the return loss at the port while varying the feature size of the joint point. Varying the connection feature size until the optimum return loss is achieved.
